Information for S3 Chipset Users

The XFree86 Project Inc.

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Contents

1 Supported hardware

The current S3 Server supports the following S3 chipsets: 911, 924, 801/805, 928, 732 (Trio32), 764 (Trio64), 864, and 964. The S3 server will also recognise the 866, 868 and 968, but it has not been tested these chipsets. If you have any problems or success with these, please report it to us.

Nevertheless, this is not enough to support every board using one of these chipsets. The following list contains some data points on boards that are known to work. If your card is similar to one of the described ones, chances are good it might work for you, too.

S3 801/805, AT&T 20C490 (or similar) RAMDAC

- Orchid Fahrenheit 1280+ VLB
- Actix GE32

8 and 15/16 bpp

Note: the AT&T20C490 RAMDAC is not automatically detected by the server. You need to provide a '`Ramdac "att20c490"`' entry in your `XF86Config`.

Real AT&T 20C490 or 20C491 RAMDACs work with the `"dac_8_bit"` option. Some clones (like the Winbond 82C490) do not.

S3 805 VLB, S3 GENDAC (RAMDAC + clock synthesizer)

- MIRO 10SD (available for VLB and PCI) It is not known whether all 10SDs use the S3 GENDAC.

8 and 15/16 bpp

```
ClockChip "s3gendac"
RamDac    "s3gendac"
```

S3 801/805, AT&T 20C490 RAMDAC, ICD2061A Clockchip

- STB PowerGraph X.24 S3 (ISA)

8 and 15/16 bpp

Note: the AT&T20C490 RAMDAC is not automatically detected by the server. You need to provide a '`Ramdac "att20c490"`' entry in your `XF86Config`.

```
ClockChip "icd2061a"
RamDac    "att20c490"
Option    "dac_8_bit
```

S3 805, Diamond SS2410 RAMDAC, ICD2061A Clockchip

- Diamond Stealth 24 VLB

8 bpp only.

requires '`Option "nolinear"`'

S3 928, AT&T 20C490 RAMDAC

- Actix Ultra

8 and 15/16 bpp

Note: the AT&T20C490 RAMDAC is not automatically detected by the server. You need to provide a '`Ramdac "att20c490"`' entry in your `XF86Config`. Also, the server's RAMDAC probe reportedly causes problems with some of these boards, and a RamDac entry should be used to avoid the probe.

Real AT&T 20C490 or 20C491 RAMDACs work with the `"dac_8_bit"` option. Some clones (like the Winbond 82C490) do not.

S3 928, Sierra SC15025 RAMDAC, ICD2061A Clockchip

- ELSA Winner 1000 ISA/EISA ("TwinBus", not Winner1000ISA!!)
- ELSA Winner 1000 VL

8, 15/16 and 24(32) bpp

Supports 8bit/pixel RGB in 8bpp and gamma correction for 15/16 and 24bpp modes

24 bpp might get "snowy" if the clock is near the limit of 30MHz. This is not considered dangerous, but limits the usability of 24 bpp.

D-step (or below) chips cannot be used with a line width of 1152; hence the most effective mode for a 1 MB board is about 1088x800x8 (similar to 2 MB, 1088x800x16).

S3 928, Bt9485 RAMDAC, ICD2061A Clockchip

- STB Pegasus VL

8, 15/16 and 24(32) bpp

Supports RGB with sync-on-green if `"sync_on_green"` option is provided and board jumper is set for BNC outputs.

VLB linear addressing now occurs at 0x7FCxxxxx so that 64MB or more main memory can be supported without losing linear frame buffer access.

Option `"stb_pegasus"`

The `"dac_8_bit"` option is always selected on this board.

S3 928, Bt485 RAMDAC, SC11412 Clockchip

- SPEA Mercury 2MB VL

8, 15/16 and 24(32) bpp

Option `"SPEA_Mercury"`
ClockChip `"SC11412"`

The `"dac_8_bit"` option is recommended.

S3 928, Bt485 RAMDAC, ICD2061A Clockchip

- #9 GXE Level 10, 11, 12

8, 15/16 and 24(32) bpp

Option `"number_nine"`

The `"dac_8_bit"` option is recommended.

S3 928, Ti3020 RAMDAC, ICD2061A Clockchip

- #9 GXE Level 14, 16

8, 15/16 and 24(32) bpp

Supports RGB with sync-on-green

Option `"number_nine"`

The `"dac_8_bit"` option is recommended.

S3 864, AT&T20c498, ICS2494 Clockchip

- MIRO 20SD (BIOS 1.xx)

The ICS2494 is a fixed frequency clockchip, you have to use X -probeonly (without a Clocks line in XF86Config) to get the correct clock values.

8, 15/16 and 24(32) bpp

S3 864, AT&T20c498 or STG1700 RAMDAC, ICD2061A or ICS9161 Clockchip

- Elsa Winner1000PRO VLB
- Elsa Winner1000PRO PCI
- MIRO 20SD (BIOS 2.xx)

8, 15/16 and 24(32) bpp

S3 864, STG1700 RAMDAC, ICD2061A Clockchip

- Actix GraphicsENGINE 64 VLB/2MB

8, 15/16 (and probably 24(32)) bpp

S3 864, 20C498 or 21C498 RAMDAC, ICS2595 Clockchip

- SPEA MirageP64 2MB DRAM (BIOS 3.xx)

8 and 15/16 bpp

ClockChip `"ICS2595"`

Clockchip support is only preliminary and on some machines problems with the first mode after startup of XF86_S3 or after switching back from VT have been seen; switching to next mode with CTRL+ALT+“KP+” and back seems to solve this problem

Mirage P64 with BIOS 4.xx uses the S3 SDAC.

S3 864, S3 86C716 SDAC RAMDAC and Clockchip

- Elsa Winner1000PRO
- MIRO 20SD (BIOS 3.xx)
- SPEA MirageP64 2MB DRAM (BIOS 4.xx)
- Diamond Stealth 64 DRAM

8, 15/16 and 24 bpp

ClockChip `"s3_sdac"` (should be detected automatically)

S3 864, ICS5342 RAMDAC and Clockchip

- Diamond Stealth 64 DRAM (only some cards)

8, 15/16 and 24 bpp

ClockChip `"ics5342"` RAMDAC `"ics5342"`

S3 864, AT&T21C498-13 RAMDAC, ICD2061A Clockchip

- #9 GXE64 - PCI

8, 15/16, 24(32) bpp

Option "number_nine"
Option "dac_8_bit" (recommended)

S3 964, AT&T 20C505 RAMDAC, ICD2061A Clockchip

- Miro Crystal 20SV

8, 15/16, 24(32) bpp

S3 964, Bt485 RAMDAC, ICD2061A Clockchip

- Diamond Stealth 64

8, 15/16, 24(32) bpp

S3 964, Bt9485 RAMDAC, ICS9161a Clockchip

- SPEA Mercury 64

8, 15/16, 24(32) bpp

Option "SPEA_Mercury"

S3 964, Ti3020 RAMDAC, ICD2061A Clockchip

- Elsa Winner2000PRO PCI

8 bpp only

S3 964, Ti3025 RAMDAC, Ti3025 Clockchip

- Miro Crystal 40SV
- #9 GXE64 Pro VLB
- #9 GXE64 Pro PCI

8 bpp, 15, 16 and 24(32) bpp

Option "number_nine"

There are some known problems with the GXE64 Pro support, including some image shifting/wrapping at 15/16/24 bpp.

We have found that #9 no longer support the GXE64 Pro at 1600x1200. They do however have a new (and more expensive) board called the GXE64Pro-1600 which uses a 220MHz RAMDAC instead of 135MHz part used on the other boards. It is not known at this stage whether the GXE64Pro-1600 will work with XFree86 3.1.

S3 764 (Trio64)

- SPEA Mirage P64 (BIOS 5.xx)
- Diamond Stealth 64 DRAM

- #9 GXE64 Trio64

 8/15/16/24 bpp

 Note: there are some display wrapping problems with the Trio64 at 8bpp which have not yet been fixed.

2 16bpp and 32bpp

On 801/805 + AT&T490 Cards (like the Fahrenheit 1280+ VLB) only 15 and 16bpp are supported. 32bpp isn't available on this type of chips. (There is a 24 bit mode under MS Windows, but it's not a 32bpp sparse mode but a real 3 bytes/pixel mode – implementing this in XFree86 isn't easy).

3 List of Supported Clock Chips

```
ICD2061A                                ==> ClockChip "icd2061a"
ICS9161A (ICD2061A compatible)          ==> ClockChip "ics9161a"
DCS2824-0 (Diamond, ICD2061A comp.)     ==> ClockChip "dcs2824"

S3 86c708 GENDAC                        ==> ClockChip "s3gendac"
ICS5300 GENDAC (86c708 compatible)      ==> ClockChip "ics5300"

S3 86c716 SDAC                          ==> ClockChip "s3_sdac"
ICS5342 GENDAC                          ==> ClockChip "ics5342"

Sierra SC11412                          ==> ClockChip "sc11412"
ICS2595                                 ==> ClockChip "ics2595"
TI3025                                  ==> ClockChip "ti3025"
```

4 Additional Notes

If you have a RAMDAC that is not listed here, be VERY careful not to overdrive it using XF86_S3. Better contact the XFree86 team first to verify that running XF86_S3 will not damage your board.

If you feel adventurous you could also open up your computer and have a peek at your RAMDAC. The RAMDAC is usually one the larger chips (second or third largest chip that is NOT an EPROM) on the board. The markings on it are usually

```
<Company logo>

    <company identifier><part number>-<speed grade>
    <manufacturing week><manufacturing year>
    <lot number><other funny numbers>
```

For example:

```
                @@
                @@ AT\&T

              ATT20C490-11
               9339S ES
                9869874
```

This is a AT&T 490 with a speed grade of 110 MHz. This would then mean that you put a '`DacSpeed 110`' line in your `XF86Config` file. Be advised that some RAMDACs have different modes that have different limits. The manufacturer will always mark the chip naming the higher limits, so you should be careful. The S3 server knows how to handle the limits for most of the RAMDACs it supports providing the DacSpeed is specified correctly.

chips labeled **-80** or **-8** should use '`DacSpeed 80`' in the device section

```
S3716-ME SDAC  ==>  DacSpeed 110
SC15025-8      ==>  DacSpeed  80
ATT20C490-80   ==>  DacSpeed  80
```

Some RAMDACs (like the Ti3025) require some mode timing consideration for their hardware cursor to work correctly. The Ti3025 requires that the mode have a back porch of at least 80 pixel-clock cycles. A symptom of this not being correct is the HW cursor being chopped off when positioned close to the right edge of the screen.

5 How to to avoid "snowing" display while graphics operations

For cards with S3 Vision864 chip there is a automatic correction which depends on the pixel clock and the memory clock MCLK at which the S3 chip operates. For most clock chips this value can't be read (only the S3 SDAC allows reading the MCLK value so far), so this value has to be estimated and specified by the user (the default is 60 MHz).

With the new '`s3MCLK`' entry for your `XF86Config` file now you can specify e.g.

```
s3MCLK 55
```

for a 55 MHz MCLK which will reduce snowing. Smaller MCLK values will reduce performance a bit so you shouldn't use a too low value (55 or 50 should be a good guess in most cases).

Below is a small shell script which might be useful to determine the approximate value for MCLK (about +/- 1-2 MHz error). Before running this script you have to add the line

```
s3MNadjust -31 255
```

to the device section in your `XF86Config` file and restart X Windows. With this option (which is for testing and debugging only) you'll get lots of disastrous display flickering and snowing, so it should be removed again immediately after running the test script below.

Running this script will use xbench and/or x11perf to run a test to determine the MLCK value, which is printed in MHz. Up to 4 tests are run, so you'll get up to 4 estimates (where the first might be the most accurate one).

```
#!/bin/sh

exec 2> /dev/null

scale=2

calc() {
  m=`awk 'BEGIN{printf "%.'$scale'f\n",'"( $1 + $2 ) / $3; exit}" `
  [ -z "$m" ] && m=` echo "scale=$scale; ( $1 + $2 ) / $3" | bc `
  [ -z "$m" ] && m=` echo "$scale $1 $2 + $3 / pq" | dc `
  echo $m
}

run_xbench() {
  r=` ( echo 1; echo 2; echo 3; echo 4 ) | xbench -only $1 | grep rate `
  [ -z "$r" ] && return
  cp="$2 $3"
  set $r
  calc $3 $cp
}

run_x11perf() {
  r=` x11perf $1 | grep trep | tr '(/)' '   ' `
  [ -z "$r" ] && return
  cp="$2 $3"
  set $r
  calc `calc 1000 0 $4` $cp
}

run_x11perf "-rect500 -rop GXxor"     3.86  5.53  #  0 1  #    4.11    5.52  #
run_xbench invrects500                4.63  5.48  #  0 1  #    4.69    5.48  #

run_x11perf "-rect500 -rop GXcopy"  -16.42 13.90  #  0 1  #  -14.99   13.88  #
run_xbench fillrects500              -7.81 13.57  #  0 1  #   -8.53   13.58  #

exit
```

```
$XConsortium: S3.sgml,v 1.6 95/01/27 16:14:30 kaleb Exp $
$XFree86: xc/programs/Xserver/hw/xfree86/doc/sgml/S3.sgml,v 3.12 1995/01/28 16:02:17 dawes Exp $
```