28 October 1994

mips
Open Risc Technology

Windows NT Update

European News on Personal Computing with MIPS Processors

Window NT: *Daytona* Imminent

- The release of Windows NT 3.5, code-named "Daytona" from Microsoft is expected within the next week. Daytona is the long awaited update to Windows NT and includes significant functional enhancements, bug fixes, and performance tuning. Availability of Daytona is expected to trigger much broader deployment of Windows NT in commercial, engineering and mission critical applications.
- Windows NT 3.5 includes Silicon Graphics OpenGL graphics programming interface. In addition, the MIPS-based systems company, NeTpower, has announced Windows NT support for Silicon Graphics Open Inventor graphics environment as well. The success of the MIPS architecture in visual computing for UNIX is clearly being carried over to Windows NT as well.
- Microsoft will be creating a new "Back Office" package to match their "Office" bundle of personal productivity tools. The Back Office package will include-Systems Management Server (code-named Hermes), Exchange Messaging Server (enhanced Microsoft Mail), SNA and SQL servers and the Windows NT Advanced Server OS components.
- The Windows NT versions of the important Office applications (Word, Excel,...) will be released 30 days after Daytona for the x86 platform, and about 90 days after Daytona for the MIPS platform. MIPS and x86 versions of Visual C++ are in the final testing stage and will be released to manufacturing this month. The DEC Alpha version will follow 30 days later.
- An updated sample of software vendors and packages now being offered on Windows NT for MIPS is shown on the back page.

T5 Sneak Preview

Fastest NT Processor on Earth

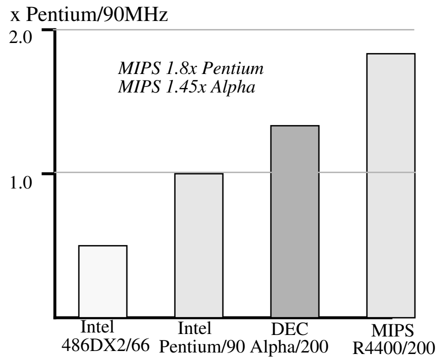
Next month, MIPS will unveil the first advanced superscalar processor targeting RISC PCs and Windows NT, code-named T5. T5 represents the start of a new family of high-performance CPUs, expected to span the systems range from large-scale multiprocessor servers down to desktops. Even the first versions will provide a factor of three performance increase over today's fastest RISC processors for general purpose Windows NT applications, and the family is expected to scale, over time, to processors with ten times the performance of today's leading desktop machines.

At the same time, T5 will provide complete application and Windows NT kernel software compatibility. The dynamic instruction issue and speculation execution features of the processor also allow existing application binaries to run at full speed without recompilation. This will allow applications to take advantage of T5 performance quickly and painlessly.

MIPS Benchmarks Windows NT

MIPS Technologies has released results from the new Application Benchmark Suite which show MIPS-based RISC PCs executing native 32-bit Microsoft Windows NT applications significantly faster than PCs based on Intel and Digital Equipment microprocessors. The tests, which include running five different scripted with real user input data, show that a MIPS-based system with the MIPS R4400 at 200MHz runs these applications up to 3.1 times faster than PCs with an Intel Pentium P54C processor at 90MHz, up to 5.5 times faster than PCs with an Intel 80486 DX-2 processor at 66MHz, and up to 1.7 times faster than a PC with a DEC Alpha AXP 21064 at 200MHz. Each of these systems is believed by MIPS to be the fastest or best configuration of PC on the market today.

Average of 5 Benchmarks



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The applications all run under the current version of Windows NT (Version 3.1). These benchmarks are based on release versions of five Windows NT applications: Texim Project from Welcom Software Technology Corporation; MaxEDS and MaxROUTE from Massteck Ltd.; PV-WAVE Advantage from Visual Numerics Inc., Image-In from CPI, Inc. and a number of iterative routines written in Hamilton C Shell. The applications span a variety of markets, including management, administration, engineering and scientific visualization. A summary of the results follows. The complete benchmark results are available from MIPS Technologies Inc.

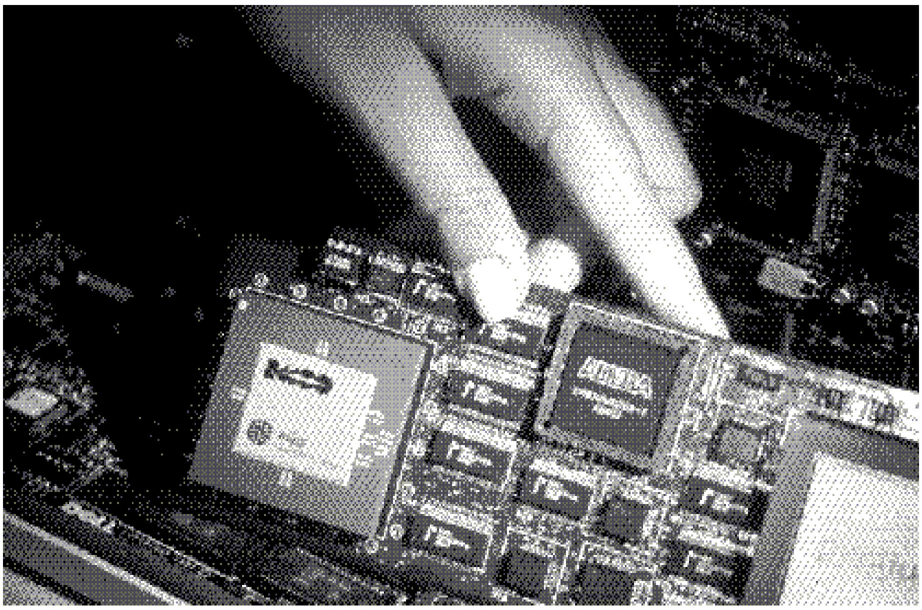
	Intel 486DX2 66MHz	DEC 21064 200MHz	MIPS R4400 200MHz
Texim Project	0.53	1.10	1.61
MaxEDS	0.56	1.86	3.08
PV-Wave	0.54	1.03	1.62
Hamilton C Shell	0.49	1.27	1.82
Image-In	0.52	1.12	1.28
Geometric Mean	0.53	1.25	1.80

TABLE 1. Performance of Windows NT Applications relative to Intel Pentium/90MHz

UltraP: Pentium - MIPS Upgrade

The new UltraP reference platform, offered through MIPS Technologies Inc. Provides PC manufacturers and users with a simple upgrade path from their existing Pentium-based systems running Microsoft's Windows operating system to high performance MIPS processor-based systems running the Windows NT operating system. PC vendors can use this design to build custom modules, using the MIPS R4600 or MIPS R4400 microprocessors, that are plug-compatible with a Pentium microprocessor. PC vendors manufacturing Pentium systems now have an option of providing to their customers, ex-factory, standard Pentium systems or upgraded higher performance MIPS-based systems without giving up the Pentium (Windows and DOS) environment. Alternatively, PC vendors can easily upgrade existing Pentium-based systems in the field to MIPS-based Windows NT systems. Preliminary benchmarking results indicate that UltraP systems running MIPS R4600 at 150 MHz deliver up to 3.5 times the performance of Pentium 66MHz and over 2.5 times P54C 100MHz systems.

The UltraP architecture uses translation logic that converts a MIPS R4600 system bus into a Pentium bus, so that the low-cost, high-performance MIPS processor can directly replace the Pentium. All interface with the motherboard system chipset remains untouched, so the existing secondary cache, main memory, graphics expansion bus and peripheral cards are untouched. In fact, the Pentium processor can remain in the system, so that the system is easily switched, in software between running Pentium software and MIPS Windows NT software. At system start-up time, the Pentium and R4600 processors are reset simultaneously. The Pentium runs all system start-up and initialization tasks and brings up DOS. At this point, the user selects Windows NT on MIPS, Windows NT on Pentium, or Windows on Pentium. If the user selects Windows NT on MIPS, system control passes to the MIPS R4600. This gives the user access to the advanced environment for networking, multi-tasking and security of Windows NT, and to the unrivaled performance of the MIPS processor. At the same time, compatibility with existing Windows applications is maintained via Windows NT's robust Windows emulator, or by rebooting with Windows running on the Pentium processor.



User installs UltraP module in Pentium-based system

UltraP Offer

MIPS Technologies has an UltraP demo unit available in Germany for benchmarking and evaluation. The module is already installed in a Dell Omniplex 566 Pentium system, with Windows and Windows NT pre-loaded. If you are interested in making an evaluation of this technology, please contact MIPS Technologies Europe (tel +41 38 433 644, fax +41

ShaBLAMM! Computers of California has already introduced the UltraP module as the "P5 detoNaTor". They can be reached as follows:

Contact:Joel Scheinberg
21040 Homestead Rd., Ste 201
Cupertino, CA 95014-0238
USA
tel +1 408 730 9696
fax +1 408 730 4940

Hardware Update: New MIPS Chipsets

In the past few months a number of new chipsets for low-cost chipsets and Windows NT RISC PC reference designs have reached the market. These represent the third generation of MIPS-based RISC PC chipsets. They typically feature lower costs, lower chip counts, more sophisticated secondary cache controllers, more efficient memory controllers and support of the latest expansion buses, like PCI. Here is a summary of the recent offerings:

Toshiba Tigershark

. R4400PC/R4600
. 2 chip bridge (i_cntlr, c_cntlr) from 64b MIPS SysAD bus to 486 local bus
. Includes L2 cache controller
. Use in conjunction with standard 486 system chip set (e.g. Opti 82C496)

Contact: Heiner Tendyck
Toshiba Electronics Europe GmbH

Hansaallee 181
D-40549 Duesseldorf
Germany
tel +49 211 5296 275
fax +49 211 5296 404

Toshiba Mako

. R4400PC/R4600
. 1x Address Control Chip (ACC) + 2x Data Path Chip (DPC)
. Includes L2 cache control, memory control and PCI interface

Contact: see above

NEC RAB^{2}IT

. RABBIT-MEMC and RABBIT-IOC
. L2 cache/memory controller (for async and sync DRAM)
. Bridge to 486 local bus
. Recently announced: RABBIT-BRAC replaces RABBIT-MEMC for RAMBUS DRAM-based systems.

Contact:Axel Kleinpaul
NEC Electronics GmbH
Oberrather Strasse 4
D-40472 Duesseldorf
Germany
tel +49 211 65 03 242
fax +49 211 65 03 344

NKK PC Design Kit:

. R4600 with L2 cache
. ND4600-MEC (Taurus) memory controller
. ND4600-BRG (Libra) CPU and PCI bus controller
. Baby AT gerber data
. System ROM (AMI BIOS)
. Windows NT HAL
. Chipset demonstrated at PC Expo in the US in June

Contact:Tracy Garnier
NKK America Inc.
2350 Mission College Blvd.
Suite 380
Santa Clara CA 95054
tel +1 408 982 8277
fax +1 408 982 9809

Deskstation LogicCore

. Three chips: cache controller, memory controller and bus-interface controller.
. Supports R4200, R4400 and R4600 at speeds up to 200MHz
. 128b secondary cache support up to 2MB
. Design kit with complete schematics, gerber, PAL equations, BOM, AVL, design guide, BIOS binaries and HAL modifications.
. Supports ISA, EISA, VESA and PCI peripherals

Deskstation Technology
Contact:Mark Lewis
James House
27/35 London Road
Newbury, Berkshire RG13 1JL
England
tel +44 773 829 542
fax +44 773 820 206
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Acer PICA I, PICA II

. Acer has been leading source for MIPS-NT chipsets
. and boards in Asia and US. The original PICA I
. Chipset consists of the following:
. 1x M6101 cache and CPU controller
. 2x M6103 buffers
. 1x M6109 I/O cache and bus controller
. 1x M6105 memory controller
. 2x M6107 data buffers
. They have recently announced PICA II which offers more
. performance at lower price and chip count.

Contact:Wim Van Seters
Hastelweg 250
Eindhoven 5652 CN
The Netherlands
tel +31 40 50 1234
fax +31 40 52 9124
.

Mentor Arc WINset

. WINset consists of three chips:
. 64C257 cache and memory controller
. 64C229/64C239 data bus chips
. 64C226 local bus to ISA bridge
. Includes L2 cache control of R4200/R4400PC/R4600
. Versions for both VL and PCI local bus

Contact:Mentor Arc
46500 Fremont Blvd. #706
Fremont CA 94538
tel +1 510 656 0100
fax +1 51- 656 3246

Background:

MIPS RISC Family

MIPS Technologies, Inc., a subsidiary of Silicon Graphics, offers world-class microprocessor performance across a broad range of applications with a highly scalable RISC architecture and open business model. MIPS currently offers three product families: the R3000 family, the R4000 family and the superscalar RISC family.

MIPS Technologies Inc. provides the industry's broadest range of processor performance by focusing on what it does best -- microprocessor design. These designs are licensed to semiconductor partners (NEC, Toshiba, IDT LSI Logic, NKK, Siemens) who fabricate and market MIPS microprocessors. The MIPS processor product line includes both standard processors, such as the R4400 and R4600, which are manufactured by multiple partners, and derivative products, such as the IDT R3051, designed to fit specific market needs. The open model creates competition between chip suppliers, and offers system makers the advantage of secure supply, low prices and constant innovation. Only the flexible MIPS Open RISC business model is capable of providing optimal price/performance solutions for the full range of processor applications from video games to supercomputers.

The small die area, low power requirements, and high performance of MIPS R3000 and R4000 family CPU cores make them ideal for new performance-hungry consumer applications such as video games and TV set-top boxes. MIPS processors are being used by companies such as Nintendo, Sony and Time-Warner to enable a new generation of home entertainment applications.

MIPS processors are currently used in a wide range of demanding embedded applications, including printers, copiers, X Windows terminals, graphics accelerators, disk controllers, LAN routers and ATM switches and emerging consumer markets. The MIPS R3000 core, with its scalability and performance is the basis for a wide range of embedded processor products, from the LSI Logic R33000 family of configurable ASICs to the HDL Systems MR300, a fully synthesizable R3000 micro-core. R4000 family derivatives will soon provide even higher performance for embedded applications.

Balanced integer and floating point performance make MIPS processors ideal for a wide range of desktop computing platforms, from Windows NT PCs to high-performance graphics workstations. In fact, MIPS currently offers the broadest line of Windows NT capable processors. These include the low-power/low-cost R4200 for portables, the R4600 for desktops, and the R4400 for high-performance servers.

Unparalleled symmetric multiprocessing capabilities and balanced integer/floating point performance are hallmarks of MIPS high-end processor, the R4400 and R8000. Silicon Graphics Challenge server, based on the R4400, recently recorded the industry's best transaction processing performance. The R8000, the first of the new superscalar computing family, is today's fastest supercomputing processor, achieving more than 300 SPECfp per processor. The MIPS tradition of processor performance leadership continues with T5, the first single-chip member of the superscalar family, which will sample in late 1994.

Technology Feature: The MIPS R4600

Introduction

The R4600 is a new CPU design that retains complete hardware and software compatibility with the R4000 and R4400 CPUs, as well as with the new low-power, low-cost R4200. It uses the same pin-out as the R4200, R4000PC and R4400PC, so that processor module redesign is trivial. It makes a number of important optimizations in internal design to enhance performance and reduce cost relative to earlier members of the R4000 family. The R4600 brings new performance levels low-cost MIPS-based systems. It does this by providing significantly higher clock rate than previous 32b MIPS CPUs, like the MIPS R3000, and larger two-set-associative on-chip caches, fewer pipeline stalls, and more efficient cache misses than previous 64b MIPS CPUs, like the R4000. Figure 1 shows a floorplan diagram of the R4600.

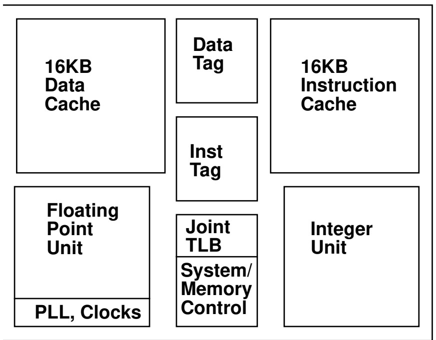
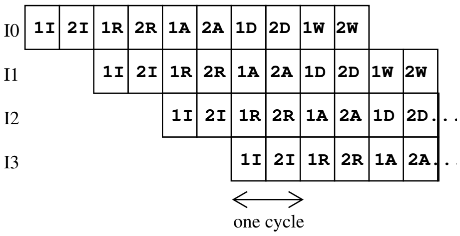


Figure 1: R4600 Floorplan

The R4600 uses a five-stage pipeline similar to the MIPS R3000. R4600 uses a simple pipeline with minimal penlites (one cycle each for branch or load-use) and makes it run as fast as possible. No superscalar or superpipeline techniques are used. Unlike the R3000, the R4600 does virtual-to-physical translation in parallel with cache access. This allows the R4600 to operate at twice the frequency of the R3000 and to support a larger TLB for address translation. In one concession to complexity, the system interface is designed to return the requested word first on a cache miss; the CPU is able to continue as soon as the word is received. Compared to the eight-stage R4000 pipeline, the R4600 is more efficient (requires fewer stalls). Figure 2 shows the R4600 pipeline.



1I-1R	Instruction cache access
2I	ITLB instruction address translation
2A-2D	Data cache access and load align
1D	DTLB data address translation
1D-2D	JTLB data address translation
2R	Register file read
2R	Bypass calculation
2R	Instruction decode
2R	Branch address calculation
1A	Issue or slip decision
1A-2A	Integer add, logical, shift
1A	Data virtual address calculation
2A	Store align

Integer Unit

The R4600 integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and autonomous multiply/ divide unit. The register resources include: 32 general purpose orthogonal integer registers, the HI/LO result registers for the integer multiply/divide unit, and the program counter. In addition, the on-chip floating-point co-processor adds 32 floating-point registers, and a floating-point control status register.

Integer Multiply/Divide

The R4600 uses the floating-point unit to perform integer multiply and divide. The results of the operation are placed in the HI and LO registers. The values can then be transferred to the general purpose register file using the MFHI/ MFLO instructions. Table 1 below shows the number of processor internal cycles required between an integer multiply or divide and a subsequent MFHI or MFLO operation, in order that no interlock or stall occurs.

Operations	R4600		R4000	
	32-bit	64-bit	32-bit	64-bit
MULT	10	12	10	20
DIV	42	74	69	133

Floating-Point Unit

The FPU handles all functions through a single non-pipelined unit. It is broken into a separate multiply unit and a combined add/convert/divide/square-root unit. Overlap of multiplies and add/subtract is supported. The multiplier is partially pipelined. Adds and similar functions take 4 cycles; multiplies take a total of 8 cycles, 6 in the multiplier and 2 in the main unit for rounding. Divides and square roots are calculated in the main unit one bit per cycle. At the peak rate, a new multiply/add combination can be launched every 6 cycles. This is somewhat slower than an R4000, which can launch a multiply/add every 4 cycles. Table 2 below shows the number of internal cycles required for the major floating-point operations.

Cache Memory

In order to keep the R4600's high-performance pipeline full and operating efficiently, the R4600 incorporates on-chip instruction and data caches that can be accessed in a single processor cycle. Each cache has its own 64-bit data path and can be accessed in parallel. The cache subsystem provides the integer and floating-point units with an aggregate bandwidth of 1.6GB per second at a pipeline-clock frequency of 100MHz.

Instruction Cache

The R4600 incorporates a two-way set associative on-chip instruction cache. This virtually indexed, physically tagged cache is 16KB in size and is protected with word parity.

	R4600		R4000	
Operations	Single	Double	Single	Double
ADD	4	4	4	4
SUB	4	4	4	4
MUL	8	8	7	8
DIV	32	61	23	36
SQRT	31	60	54	112
CMP	3	3	3	3
FIX	4	4	4	4
FLOAT	6	6	2	4
ABS	1	1	2	2
MOV	1	1	1	1
NEG	1	1	2	2
LWC1, LDC1	2	2	3	3
SWC1, SDC1	1	1	1	1

Because the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, thus further increasing performance by allowing these two operations to occur simultaneously. The tag holds a 24-bit physical address and valid bit, and is parity protected.

Instruction cache is 64-bit wide, and can be refilled or accessed in a single processor cycle. Instruction fetches require only 32 bits per cycle, for a peak instruction bandwidth of 400MB/sec. Sequential accesses take advantage of the 64-bit fetch to reduce power dissipation, and cache miss refill writes 64 bits per cycles to minimize the cache miss penalty. The line size is eight instructions (32 bytes) to maximize performance.

Data Cache
For fast, single cycle data access, the R4600 includes a 16KB on-chip data cache that is two-way set associative with a fixed 32-byte (eight words) line size.

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access.

The normal write policy is write back, which means that a store to cache line does not immediately cause memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each store operation to finish before issuing a subsequent memory operation. Software can however select write-through on a per-page basis when it is appropriate, such as for frame buffers.

Associated with the Data Cache is the store buffer. When the R4600 executes a Store instruction, this single-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data is written into the Data Cache in the next cycle that the Data Cache is not accessed (the next non-load cycle). The store buffer allows the R4600 to execute a store every processor cycle and to perform back-to-back stores without penalty.

Write Buffer
Writes to external memory, whether cache miss write-backs or stores to uncached or write-through addresses, use the on-chip write buffer. The write buffer holds up to four 64-bit address and data pairs. The entire buffer is used for a data cache write-back and allows the processor to proceed in parallel with memory update. For uncached or write-though stores, the write buffer significantly increases performance over the R4000 family of processors.

System Interface

The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 400MB/sec at an external clock rate of 50MHz.

Comparison with R4000PC

Table 2 and 3 highlight some of the differences in the pipeline, the cache subsystem, and the floating-point unit between the R4600 and the R4000PC. This list is not exhaustive.

TABLE 2. Pipeline comparison between R4000PC and R4600

	R4000PC	**R4600**
Pipeline	8-stage Super Pipeline	5-stage Pipeline
ALU latency	1 cycle	1 cycle
Load latency	3 cycles	2 cycles
Branch latency	4 cycles	2 cycles
Store Buffer (not write buffer)	2 doublewords	1 doubleword
Integer multiply	Integer multiply hardware, 1 cycle to issue HI and LO available at the same time	done in floating-point multiplier, 4 cycles to issue LO available one cycle before HI
Integer divide	done in integer data path adder, slips until done HI and LO available at the same time	done in floating-point adder, 4 cycles to issue HI available one cycle before LO
HI and LO hazards	yes, HI and LO written early in pipeline	no, HI and LO written after W (the write stages)
MFHI/MFLO latency	1 cycle	2 cycles
SLLV, SRLV, SRAV	2 cycles to issue	1 cycle to issue
DSLL, DSRL, DSRA, DSLL32, DSRL32, DSRA32, DSLLV, DSRLV, DSRAV	2 cycles to issue	1 cycle to issue

TABLE 3. Cache comparison between R4000PC and R4600

	R4000PC	**R4600**
Cache Sizes	8KB Instruction cache, 8KB Data cache	16KB Instruction cache, 16KB Data cache
Cache Line Sizes	software selectable between 16B and 32B	fixed at 32B
Cache Organization	direct mapped	2-way set associative
Data cache write policy	write-allocate and write-back	write-allocate or not based on TLB entry, write-through or not based on TLB entry
Data cache miss	stall, output address, copy dirty data to write-back buffer, refill cache, output writeback data	same, with FIFO to select the set to refill
Data cache miss restart	restart after all data received and written to cache	restart on first doubleword, send subsequent doublewords to response buffer
Instruction Tag	2-bit cache state	1-bit cache state
Cache miss overhead	5-8 cycles	3 cycles
Instruction cache parity	1 parity bit per 8 data bits	1 parity bit per 32 data bit
Data cache parity	1 parity bit per 8 data bits	same

The R4600 uses 16KB instruction and data caches -- the same as the R4400, and twice the size of the R4000's. In addition, it uses two-way set associativity, instead of direct mapping in the cache look-up to improve hit rates. In a direct mapped cache, the processor checks in only a single location for a requested data or instruction item. If it is not there, it takes a cache miss and looks outside the processor. In a two-way set-associative cache, the processor looks in two locations in the on-chip cache. The processor must look off-chip only if the requested item is in neither of the two locations. This significantly improves the hit rates and improves the average execution time. In fact, a 16KB two-way set-associative cache typically has a hit rate that is almost as good as a 32KB direct-mapped cache. Clever design of the cache circuitry allows associative caches without any penalty in clock frequency.

The R4600 reduces the overhead for primary cache misses. Even though it does not include a private secondary cache interface, its low latency main memory interface allows low miss penalties and high sustained performance even on applications with significant cache miss rates. Moreover, the main memory interface is sufficiently flexible to allow a simple secondary cache to be added to the system design with little increment design effort or cost at a later time.

In many cases the R4600 is replacing the R4000PC, the first 64b MIPS processor for low-cost systems, primarily because of strong performance and lower manufacturing cost than the R4600. The R4600 costs are lower for four reasons:

1 The design has been optimized for the 0.64 micron process used for fabrication, unlike the R4000 which was design for 1.0 micron technology and later scaled to fit the 0.64 micron process.

2 The design supports only uni-processor functions, so much of the multiprocessor cache coherency and synchronization control overhead of the R4000 and R4400 chips has been omitted.

3 The design omits the dedicated secondary-cache interface of the R4000 and R4400 designs, reducing the number of bonding pads on the chip from roughly 450 to about 180. Moreover, the low pin count will allow the die size to be reduced still further as 0.5 micro processes become available for volume manufacturing.

4 The simplification of the pipeline, and the reduction of the floating point overlap allow a much more compact layout of the datapaths and associated control blocks.

The combination of features allows the die size to shrink to just 75 square mm, compared to R4000 or R4400PC at about more than 180 square mm in the same generation of fabrication technology.

The design of the R4600 was done under contract by Quantum Effect Design (QED), with cooperation and verification by MIPS Technologies. The current vendors, IDT, Toshiba and NKK have announced and demonstrated 100, 133 and 150 MHz versions.

Technical Background: MIPS R4200

- Performance:SPECint92 55 SPECfp92 30
- Power dissipation:Full-on mode: 1.5 watts
- Reduced power mode: 0.4 watts
- Power-down mode0 watts
- Packaging:R4200LP 208-pin Plastic Quad Flat Pack R4200PC 179-pin Ceramic Pin Grid Array
- Clock frequency:External/ Internal 40 MHz / 80 MHz
- Die size:8.8 mm x 8.6 mm
- 1.3 million transistors
- Process Technology:0.6 micron, three-level-metal CMOS

Overview

This paper introduces the RISC R4200 microprocessor from MIPS Technologies, Inc. The information presented in this paper discusses how the R4200 differs from previous microprocessors from MIPS. This chapter provides general information on the R4200, including the R4200 microprocessor -The portable4000 family, packaging and design support and future upgrades.

Introduction

Reduced instruction-set computer (RISC) architectures differ from older complex instruction-set computer (CISC) architectures by optimizing performance for the available silicon area. The MIPS architecture, developed by MIPS, is firmly established as the leading RISC architecture to-day.

The MIPS R4200 microprocessor extends the benefits of RISC's speed to portable computing. The R4200 microprocessor also delivers high performance to existing embedded and computing applications at a low cost. The low cost and high performance provided by the R4200 are needed for the latest generation of operating systems, such as Windows NT.

In the past, RISC microprocessors have been fast but expensive and limited to higher power applications. However, new applications are embracing RISC and low- cost parts are appearing. The R4200, for example, can deliver up to 55 times the integer performance of a VAX 11/780 (55 SPECint '92) at a cost approaching $1 per SPECint by 1995. The R4200 also consumes less than 1.5 watts. Lower power dissipation allows the use of low-cost plastic packaging. This makes the R4200 a strong candidate for both system processing and embedded applications.

Between 1985 and 1993, three generations of the MIPS architecture have been introduced and widely adopted. The first commercial MIPS processor, the R2000, ran at 8-MHz and used a 32-bit architecture. The R3000 family raised system speed to 40 MHz. The R4000 family uses a 64-bit architecture to boost instruction throughput and increase the available address space. It also adds multilevel cache and multiprocessor capabilities. The R4000 family (R4400PC, R4400SC, R4400MC, R4000PC and R4000SC) also supports pipeline speeds of up to 150 MHz.

MIPS's semiconductor partners have successfully implemented a variety of semiconductor processes for MIPS processors including CMOS, Gallium Arsenide (GaAs) and Emitter Coupled Logic (ECL) and introduced numerous derivative products. MIPS semiconductor partners include Integrated Device Technology, Inc., LSI Logic Corp., NEC Corporation, Performance Semiconductor, Inc., Siemens and Toshiba Corporation. Users of the MIPS architecture include AT&T, Control Data, Digital Equipment Corporation, NEC, Network Computing Devices, QMS, Siemens- Nixdorf, Silicon Graphics and Tektronix.

The R4200 uses a variety of techniques to provide high performance, low cost, and low power. These techniques include power-reduction features, power management features, cost-reduction features, and architectural optimizations. Major R4200 characteristics include 64-bit processing, 80-MHz internal operation from an external 40-MHz clock, low-voltage operation, power-saving modes, plastic packaging, a single data path for integer and floating-point operations, and software compatibility with all existing MIPS microprocessors. The next section provides a complete description of architectural enhancements in the R4200 over previous MIPS microprocessor families and other R4000 family members.

The R4200 is the first member of the portable4000 family of microprocessors. The portable4000 family uses power management features to bring high performance and low cost to the portable market. Future portable4000 family members are planned to increase the options available to systems developers. The R4200 has been designed in well-defined basic blocks to simplify implementation of the R4200 core logic in new products. For example, by removing the caches, memory-management unit, and system interface, a high-performance RISC core is available for integration in a derivative processor or ASIC. Packaging and Design Support The R4200 will be made available in two packages, a 208-pin PQFP and a 179-pin CPGA. The 208-pin plastic quad flat pack (PQFP) offers a low-cost package for surface- mount assembly, decreasing processor cost further to benefit embedded applications, and with a low profile suitable for notebook computers. The 179-pin ceramic pin-grid array (CPGA) provides a compatible pin-out with existing R4000PC and R4400PC designs.

An R4200-based design kit has been announced for future availability by MIPS's Open Design Center (ODC). The ODC is an open research and development facility to help personal computer manufacturers build low-cost MIPS RISC-based personal computers running Microsoft Windows NT. The ODC plans to offer a design kit for systems priced less than $2,000 called the portable riscPC design kit. The portable riscPC design kit will be based on the R4200. Future Upgrades It is anticipated that higher frequency versions of the R4200 will become available in the future. These will provide an extra performance boost at the same low price points as the current R4200.

Implementation

When compared to previous R4000 family members, there are four main categories of new or different features in the R4200. These categories, discussed in the next sections:

- Power reduction features
- Power management features
- Cost reduction features
- Architectural optimization

These features combine to achieve typical power dissipation of 1.5 watts, a reduced power mode dissipation of 0.4 watts, and a power-down mode where the processor is turned off. These features also allow a die size of approximately 9mm on a side, while maintaining full 64-bit operation

. Power Reduction Features

The R4200 is designed using low-power design techniques. These are techniques that reduce power dissipation while running standard tasks. Examples of low-power design techniques, discussed below

- 3.3-Volt operation
- Dynamic logic design
- Cache bank partitioning
- Write-back data cache
- Cache prefetching
- Micro TLB

3.3-Volt operation

Most microprocessors now in production use a 5-Volt power supply. The R4200 was designed for operation at 3.3V. CMOS power dissipation increases with the square of potential difference between power (VDD) and ground (VSS). At lower voltage levels, however, the threshold voltage at which a logic signal switches between zero to one changes. Redesign of the gate's physical width-to-length ratio is necessary to maintain logic speed at lower voltages; that slightly increases total power dissipation. In sum, reducing the rail-to-rail voltage difference by 1.7 volts reduces overall comparative power dissipation to about 70%. A lower rail-to-rail (VDD to VSS) voltage difference also increases the chip's sensitivity to electrical noise, as there is a smaller noise margin around the threshold voltage. MIPS designed the R4200 interface using low-voltage CMOS (LVCMOS) characterization to ensure noise immunity and reliable signal operation.

Dynamic logic design

The R4200 uses dynamic rather than static logic design to reduce transistor count and dissipated power. Static designs have been used in the past to allow a processor's clock to be slowed to 0 Hz, a capability not judged useful to the R4200. The R4200's power management functions make the dynamic logic design approach suitable for use in portables.

Cache bank partitioning

Most instruction and data cache accesses are sequential. In the R4200, the instruction and data caches are each split into four banks; only one of the four banks in the instruction or data caches is powered up at any one time. This saves power on every cache access cycle. There is no performance degradation on cache bank misses; enabling of cache banks is entirely transparent to system operation.

Write-back cache

Older cache architectures used a write-through cache mechanism. Write-through caches change data in main memory every time any item in the cache changes. The R4200 instead uses a write-back cache; cache data is only written back to main memory when new data is fetched into the cache from main memory. Write-back caching reduces store activity on the system bus, which improves system performance and simplifies memory subsystem design.

Cache prefetching

As instruction reads are usually sequential, the R4200 fetches two consecutive 32- bit words (instructions) every time it reads the instruction cache. Dual instruction access from the cache reduces the frequency of cache enabling for instruction access, which reduces power dissipation.

Micro Instruction-TLB

The memory management unit (MMU) translates virtual addresses to physical addresses by looking up address correspondences in a "page table". The processor maintains a complete page table in main memory, but accesses to main memory are slow. The translation lookaside buffer (TLB) keeps copies of page table entries on- chip, which accelerates virtual-to-physical address translation. The TLB structure is large and consumes power when enabled. The R4200 therefore includes a "micro TLB" on chip which contains page table entries for the two most recently referenced instruction pages. The micro TLB eliminates a large number of main TLB accesses.

Power Management Features

As well as power reduction features, the R4200 also has built-in power management features. Power management lets the processor enter power reducing modes when peak performance is not required. These modes require less power and therefore reduce average power consumption over a period of time, extending battery life in portable applications. The power management modes are discussed below:

- Standard operating mode
- Reduced power mode
- Power-down mode

Standard operating mode

In this mode the processor operates at a maximum of 80 MHz pipeline speed and 40 MHz external interface speed. Power dissipation at maximum frequency in this mode is estimated at 1.5 watts.

Reduced power mode

This feature allows the processor to change dynamically to one quarter of the normal speed. The pipeline then operates at 20 MHz, and the system interface at 10 MHz. Typically, chipset logic triggers this mode when it detects no user activity (such as between keystrokes or mouse movements). In reduced power mode, power dissipation falls to 0.4 Watts, one quarter of the normal.

Power-down mode

In the R4200, all variable registers are both readable and writable. On power-down, the state of the processor can therefore be written to non-volatile RAM. On power-up, the registers can be restored to the same state. This “instant-on” capability allows the processor to be activated in milliseconds, instead of the many seconds normally required to boot an operating system. This not only reduces power consumption but is an essential feature for portable computers.

Cost Reduction Features

The R4200 is designed to be highly manufacturable at low cost. The three main areas contributing to microprocessor cost are packaging, test and assembly, and die costs. The designers lowered costs in all three areas but particularly reduced die size, where size reduction would not significantly impact overall performance.

Packaging cost reduction

For low cost applications, the R4200 will be available in a plastic quad flat package (PQFP). High-performance microprocessors normally require expensive ceramic or metal packages with enhanced thermal dissipation because of their higher power requirements.

Test & assembly cost reduction

The R4200 implements column redundancy in both instruction and data caches. Column redundancy reduces the chip’s sensitivity to defects in the caches; caches necessitate densely placed features during processing, which raises the likelihood of defects impacting logic integrity in the cache areas. The test process first tests the integrity of each bit column in the cache; polysilicon fuses in the chip are then blown to swap redundant bit columns for defective bit columns. Column redundancy increases the die yield at the test stage, which in turn decreases testing costs for each good die.

Die cost reduction

The die area was reduced by the following techniques:

- High-density 0.6 micron design rules
- Use of 4-transistor RAM cells in the caches
- Unified CPU/FPU data path
- Reduced configurability
- Optimized cache and TLB size

The last three cost reduction strategies fall in the category of architectural optimizations, discussed below.

Architectural Optimizations

The R4200 is a completely new design. However, in the interests of compatibility, the R4200 only differs a little from the R4000 microprocessors. In particular, the R4200 fully implements the current ISA, MIPS-III standard. As in all the MIPS R3000 and R4000 processors, an on-chip CP0 coprocessor contains an MMU for virtual address translation and exception processing control. The system address/data bus interface is identical with that of the R4000 series processors, with full 64-bit address and data paths. A flush buffer, which was added to the R4400 for increased graphics performance, is retained in the R4200.

The R4200 also includes on-chip clock frequency division circuitry to support internal 80-MHz operation from an external 40-MHz clock. This allows high microprocessor performance and also simplifies system design. The differences from the R4000, discussed below,

- Combined integer/floating-point data path.
- Optimized 5-stage pipeline
- Optimized cache and TLB size
- Reduced configurability
- Reduced physical address space
- Additional instruction trace support
- Simplified processor initialization

Unified integer/floating-point data path

The R4200 uniquely possesses a CPU unit which shares its data path with the FPU unit. CPU and floating-point instructions are both executed in the same 5-stage pipeline. This represents a considerable saving in die area and corresponding power dissipation.

Optimized pipeline

Pipelining allows multiple instructions to overlap during execution for greater throughput. All processor operations require five basic operations: instruction fetch, instruction decode, instruction execution, accessing data and writing of the results. These operations can be split up over a pipeline so that several instructions can be treated concurrently: while one instruction is being decoded, another can be fetched, and soon. The R4200 uses a five-stage pipeline instead of the eight-stage pipeline found in the R4000 series processors. The eight-stage pipeline allows the R4000 series processors to reach higher speeds. However, the shorter pipeline achieves greater efficiency at a given speed than its longer counterpart. Loads, stores, jumps and branches are resolved in fewer cycles, and exception processing is simplified. Less control logic means reduced die area. Optimized cache and TLB size As in the other R3000 and R4000 series processors, the R4200 uses separate instruction and data caches. Instruction cache size impacts performance to a greater extent owing to locality of instruction code. The combination of 16-Kbytes instruction cache and 8-Kbytes data cache gives optimum performance for a fixed total cache size. The on-chip TLB is also reduced from the 48 entry-pairs in the R4000 to 32 entry- pairs. These sizes have been selected after extensive simulation to give the R4200 the best trade-off between high performance and small die area.

Reduced configurability

As it is targeted at low-cost systems, die area is reduced by removal of functions that are not crucial. The R4200 uses a fixed divide-by-two clock division, rather than variable clock division, for example. The system bus has also been simplified by removing support for multiple processors and secondary caches. In addition, only 4-Kbyte and 16-Mbyte virtual page sizes are supported, instead of the seven different virtual page sizes supported in the R4000 series processors. Reduced physical address space The physical address space has been reduced from 36 bits to 33 bits. This still supports a physical address range of 8 Gbytes, more than enough for low-cost and portable systems.

Additional instruction trace support

The R4200 includes an additional debugging mode called instruction trace support. This mode lets the user find out the physical address to which the CPU has branched or jumped whenever a branch, jump, or exception is taken. This is a new debugging facility not available in previous implementations of the MIPS architecture. Simplified processor initialization Processor initialization has been simplified, reflecting the lower degree of configurability. The R4000 processors require loading of registers during initialization, accomplished via an on-chip register loading facility that clocks an off-chip serial PROM. On the R4200, a number of configuration options are simply hardwired.

Benefit Summary

The main benefits of the R4200 are improved price/performance, low power operation and MIPS processor family compatibility.

Price/Performance
The R4200 dramatically improves price/performance for both system designers and end-users. Although a number of RISC architectures have succeeded in pushing through the 50 SPECint barrier, all leading processors cost close to $1,000 on introduction. The R4200 achieves price/performance ten times better than existing microprocessors. The R4200 may be the first commercially available processor to approach the $1/SPECint mark by 1995.

Low Power
The R4200 was specifically designed for battery-powered devices by including both reduced power and power management features. Reduced-power features are those that perform traditional tasks in a way that reduces energy consumption. Power management features are architectural enhancements that further reduce internal and system-wide power consumption through switching modes. The combination of reduced-power and power-management features allows the R4200 fit in an inexpensive plastic package.

Low Cost
In practice, good price/performance usually means increased performance at a given price point. The R4200, in contrast, brings existing high-performance levels to an unprecedented low price-point. System manufacturers can decrease component costs, thereby increasing margins, or offer their products at a lower price, thereby stimulating demand. Price-sensitive embedded applications such as X-terminals, laser printers, graphics, and networking benefit particularly from a low cost, high-speed microprocessor. Factory automation and robotics are also likely applications for the R4200.

Compatibility
Software compatibility is a fundamental requirement to preserve investments in software and data, through time. All MIPS processors maintain software compatibility. A program compiled and linked to run on the first MIPS processor will run on the R4200 in an identical manner. The R4200 also maintains hardware compatibility with the MIPS R4000 family members. Although the R4200 is a completely new design, many R4000 family features (such as 64-bit addressing, multiplexed system interface, and virtual address translation) have been retained. The hardware compatibility yields two benefits:

1 The design cycle is shortened for system designers familiar with the R4000.

2 Low-level hardware-dependent software (such as shrink-wrapped Windows NT) can run unchanged on the R4000, R4400 and R4200 (processor-specific differences are masked by the Hardware Abstract Layer (HAL)).

The R4200PC has an R4000PC-like pin-out, making it possible for a single design to use either processor.

A MIPS Glossary

ARCS
(Advanced RISC Computing Specification) The reference platform for Microsoft's Windows NT on MIPS microprocessors.

Cache
An on-chip temporary storage area containing a copy of main memory fragments. Cache access is much faster than main memory access.

CISC
(Complex Instruction Set Computing) A design approach that attempts to achieve performance gains with complex instruction and data types and hardware controlled memory management.

CPGA
(Ceramic Pin-Grid Array) A ceramic package with a grid of pins, instead of only having pins around the edge.

CPU
(Central Processing Unit) The part of a microprocessor where the majority of the instructions are executed.

Die
The silicon chip after it has been cut from a wafer and before it has been packaged.

DSP
(Digital Signal Processing) An instruction stream which manipulates digital data, generated, for example, from sound or video. Requires intensive addition and multiplication of 8-bit or 16-bit quantities, often implemented in dedicated hardware.

Flush Buffer
(sometimes called a write buffer) The flush buffer is a temporary storage location for data that is being written from the pipeline or cache to main memory. The flush buffer allows the processor to continue executing instructions while data is being written to main memory.

FPU
(Floating-Point Unit). Dedicated logic to accelerate calculations using floating-point numbers.

IU
(Integer Unit). The part of a CPU that performs calculations using integer arithmetic.

LVCMOS
(Low-voltage CMOS). An IEEE standard for low-voltage logic interface design.

MMU
(Memory Management Unit). That part of a microprocessor which implements virtual-to-physical address translation and the memory system hierarchy including cache memory.

MIPS
(MIPS Technologies, Inc.) The developer of the MIPS RISC architecture, the leading RISC architecture worldwide.

ODC
(Open Design Center) An MIPS research and development facility to help personal-computer manufacturers easily build low-cost PC's running Microsoft Windows NT.

MPU
(MicroProcessor Unit) The combined CPU, MMU, and FPU facilities in a computer system.

Page Table
An area of main memory containing sets of virtual addresses with their corresponding physical addresses and protection data. The TLB serves as an on-board cache of page table entries.

RISC
(Reduced Instruction Set Computing) A design philosophy that avoids implementing complex functions in silicon but realizes large performance increases through executing simpler, standardized instructions at faster, more efficient rates.

RISC-like.
A term coined by Intel to describe their x86 and Pentium processors. See CISC.

Pipeline
A mechanism to allow multiple instructions to overlap during execution for greater throughput. A five-stage pipeline offers peak performance five times that of a non-pipelined processor.

PQFP
(Plastic Quad Flat Pack) A plastic package with pins on the four edges, cheaper than a CPGA.

SL
An Intel processor family targeted to portable computers but now being dropped

because it cost more, not less, to make than DX equivalents.

TLB
(Translation Lookaside Buffer). An on-chip "page table" cache containing copies of the page tables used by the MMU for virtual-to-physical address translation.

32-bit Processor
A processor without 64-bit processing capabilities. 32 bit processors may include 64 bit data paths for bringing data from memory, but cannot processor more than 32b per primitive operation.

64-bit Processor
A processor in which all address and data paths are 64 bits wide. Leading-edge applications require 64-bit processors today. 32-bit capability in a 64-bit processor is important to manage the smooth transition from 32 to 64 bits. The MIPS R4000, R4400 and R4200 MPUs can run in either 32-bit or 64-bit mode.

Perspective: Open RISC Technology

Dr. Chris Rowen, Director, MIPS Technologies Europe

- Fundamental shifts in computing technology are driving significant changes in the computer and digital electronics business. These changes will create new winners and losers not only in the conventional computing business, but also across the growing range of businesses tied to communication, entertainment and office and factory equipment.

Here are the important trends:

- Price, performance and functionality of digital electronics is increasingly dominated by the price, performance and functionality of the microprocessor that serves as the heart of the product. The primary force underlying this trend has been the phenomenal improvement in processor performance and price/performance over the last decade. VLSI processor performance, in every price class, has been growing at a compound rate of about 60% per year. Programmable solutions have displaced special purpose digital and analog circuitry in every type of electronic device from toys to global communications networks.
- CISC (complex instruction set computer) design is dead, though Intel's x86 architecture, the last CISC, willremain for some time. No new CISC architectures have been introduced in the past ten years. The decisive advantages of RISC (reduced instruction set computer) architectures in price, performance and adaptability have led to domination in virtually every performance-sensitive market (e.g. UNIX, printers, graphics, telecommunications, games and other high-end embedded control).
- Modern application programming in high-level languages and portable operating systems like UNIX, Windows NT, Workplace OS, MacOS, and Taligent are reducing the significance of instruction set compatibility and creating the opportunity for new processors -- RISC processors -- to enter the personal computer world so long dominated by Intel's x86 architecture. The impact of new operating systems is gradual, but unstoppable. The typical ramp to establish a new operating system standard is two to three years from the time of introduction. Establishing a new microprocessor architecture follows a similar schedule, because of intrinsic delays in system development, training, software porting, and tuning. A new architectures only succeeds if it offers enough price, performance or functional advantages to justify this retooling. In the Windows NT market, for instance, RISC will be particularly attractive for high-end desktops and servers needed to realize powerful client/server and digital media-intensive applications.
- The price tag for state-of-the-art semiconductor fabrication facilities continues to grow, with the capital investment for a high-volume factory approaching $1B. These factories need a high volume of profitable parts to amortize the investment. High volume profitability comes from good performance, broad acceptance, and small die size.
- The intrinsic scalability and high volume of memory devices have combined to help CMOS-based device meet or beat the performance of devices built from more esoteric gallium arsenide, ECL or biCMOS technologies. Difficulties in building high-complexity ICs, excessive power dissipation and the unit volume punishes the manufacturers and users of non-standard CMOS technology.
- The computing industry has finally completed the painful conversion from 16 bit architectures to 32 bit architectures, but larger applications still face a crunch in addressing range. Because of the long-term drop in storage costs, the growth of distributed computing, and the advent of object-based programming, systems require a doubling in address range (adding one bit to the address size) roughly every 12 to 18 months. By 1995 a great many applications will exceed the capabilities of 32 bit addressing. Those processor, software and application architectures which have already converted to 64 bit addressing will have a natural advantage over those that still focus on a 32 bit addressing model.

These trends are bringing fundamental changes to the computer and microprocessor industry. The growth in the performance of microprocessors, especially RISC microprocessors, has rapidly undermined the value of the installed base of the traditional computer companies. IBM and Digital are both now just starting the conversion of their mainstream mainframe, AS/400 and VAX business to RISC, a process that is likely to mean several years of shrinking revenue and questionable profitability. Other companies, like Intel and Hewlett Packard recognize that their current processor designs may not have necessary extensibility to keep up with this pace, and have started to talk of moving to new architectures over the next three to five years.

The MIPS processor architecture is uniquely positioned to take advantages of these trends. The MIPS architecture, first shipped in systems in 1986, was one of the first RISCs to appear, and is the one architecture which has remained true to the RISC principles of simple instruction set encoding, applicability across a broad class of applications, portability to different process technologies and suitability to a range of pipeline and superscalar implementation methodologies. In addition, MIPS Technologies, the processor development arm of Silicon Graphics, has created the strongest partnership of semiconductor supporters in the industry, with high-performance pin-compatible chips available from five major suppliers (NEC, Toshiba, Integrated Device Technology, NKK, LSI Logic and Siemens), and more than 25 different processor variants available to embedded applications. MIPS itself does not sell chips, but rather, architects and designs processors in leading-edge, but standard, CMOS technology, and then licenses the design to leading semiconductor manufacturers. These man-

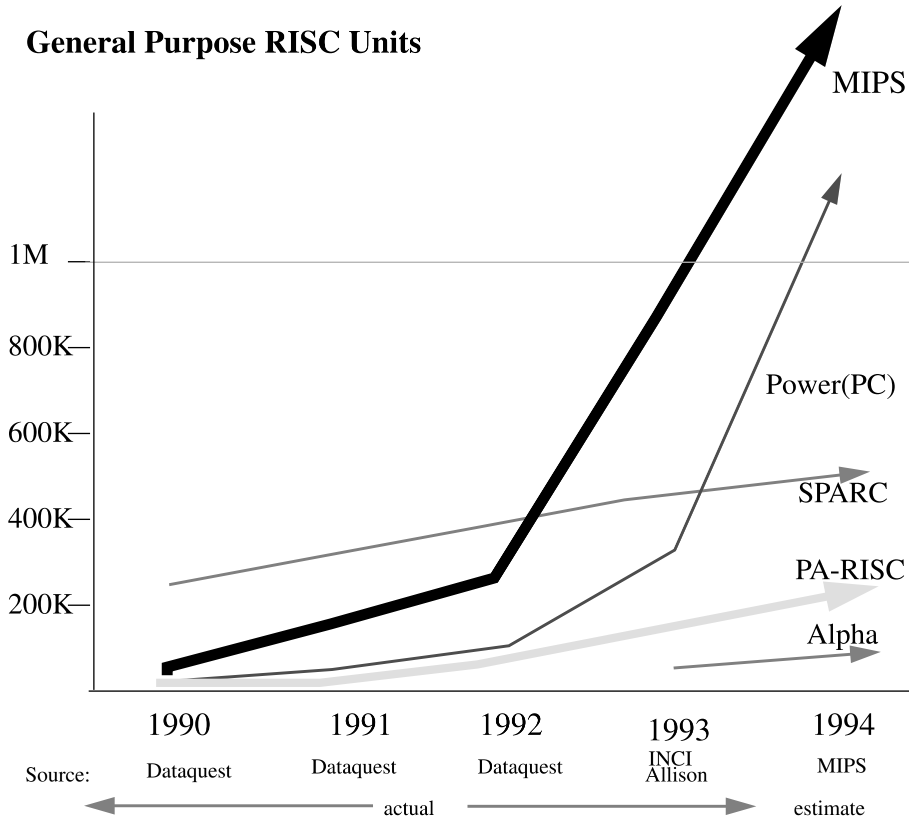


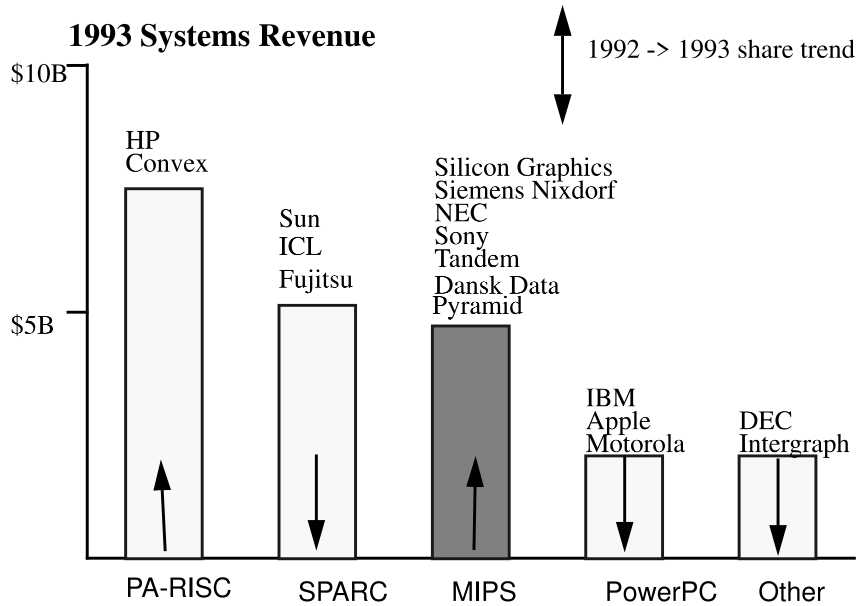
Figure 1

ufacturers build MIPS CPU in the same factories, using essentially the same technology, as they use for high volume static and dynamic RAMs, and digital logic devices. This strategy ensures that MIPS Technologies operates as a healthy business, drives down the true part cost, and creates competition among MIPS's semiconductor partners. This competition dramatically increases the attractiveness of the MIPS architecture to potential system makers, since it ensures multiple compatible sources of supply. The competition, in turn, encourages more design wins for MIPS vendors and guarantees the volume necessary to semiconductor profitability. With MIPS, the system maker gets both state-of-the-art technology, and the best long-term pricing model.

This success of this partnership model can be measured four ways, in the volume of chips, in the breadth of applications and adopters, in the proliferation of compatible CPU implementations and by the price and performance of the chips. By any of these measures, the MIPS architecture is first among all general-purpose RISC architectures. Recent history in general purpose RISC chip volume is shown in Figure 1 (Data from Dataquest up through 1992, from Inside the New Computer Industry for 1993, except PA-RISC.).

The MIPS volume is 2x SPARC, 3x Power, 5x HPPA, and 12x Alpha. Among RISC designs only the i960, used solely in embedded control applications like HP's laser printers, draws substantially more volume. The MIPS architecture has also been adopted by major system manufacturers, including NEC, Siemens Nixdorf, Tandem, Pyramid, Concurrent, Dansk Data Elektronik, and, of course, Silicon Graphics. Even though almost 75% of the MIPS chips go into various embedded applications, these manufacturers have made MIPS one of the leading system architectures, measured by revenue. The 1993 revenue by RISC architecture is shown in Figure 2 It also shows that from 1992 to 1993, only the MIPS and PA-RISC architectures gained market share. Five high-end MIPS CPU chip implementations are available and the number of compatible low-cost MIPS implementations has become difficult to track, since new versions for special applications appear almost every month. These embedded applications include high volume laser printers like Oki 400 series, the Canon color copier, The complete CISCO network router and controller family, half a dozen different high-bandwidth telecommunications switches, virtually all high-end X Windows display terminals and a wide variety of graphics and storage controllers. The price and performance position is particularly important, so it is dealt with separately below.

The MIPS business model shows an interesting contrast to that of Digital's Alpha program. Digital is only18 months into the long process of establishing Alpha, and the slow growth of the Alpha business shows how difficult it is to establish a new architecture without a compelling lead in price, performance or functionality over more established architectures. Digital has



Source: Andrew Allison, Inside the New Computer Industry, 1.94

Figure 2

attempted to establish Alpha as an open architecture standard, but without a viable second source or software base, the enthusiasm has been limited. Alpha CPUs are built with an odd CMOS variant (low threshold voltages, extra metal thickness) which makes the design virtually unbuildable outside Digital's own special fab facilities. These facilities build no other high volume DRAM, SRAM or digital logic parts, so Alpha production must carry the bulk of the capital costs. Digital CEO, Robert Palmer, has said that the break-even point for their investment in Alpha fab facilities is 4-5 million units per year. Digital has now given over much of the capacity of its South Queensferry (Scotland) fab to Advanced Micro Devices, for manufacturing of 486 clones, using a more standard fabrication process.

The MIPS model also contrasts sharply with that of Hewlett Packard. The only implementations of HP's Precision Architecture (PA-RISC) shipping today are those built by HP for internal use. HP has not sought broad acceptance of the architecture for applications outside it own UNIX workstations and servers. Its own internal fabrication capacity is limited, so the volume of HPPA chips is small (one fifth of the MIPS volume), and the processors must be implemented without on-chip caches, since HP does not have state-of-the-art static RAM fabrication technology. For the current generation of products, HP has built competitive products by pushing the limits of an off-chip cache strategy -- the HP 7150 systems, for example, require extremely fast static RAMs (less than 8ns access). In addition, HP does not yet have processor fabrication technology available below 0.8 micron in production, and the PA-RISC instruction set is comparatively complex, so the die size, even for the 7100LC is large, 196 mm^2, without on-chip caches. For comparison, the MIPS R4600, a chip at about the same performance level, built in a multi-source 0.64 micron CMOS is only 75 mm^2, of which half is devoted to caches. In the long run, in-house fabrication will probably limit PA-RISC chips to lower frequency applications where off-chip caches are viable, and to low-volume markets where chip-level price/performance is less critical. HP's recognition of this constraint has driven it into alliance with Intel, which already supplies all of the CPUs for HP's PCs and laser printers. HP and Intel will pool technology into a new chip architecture, and will attempt to move their current PA-RISC and x86 customers to this new architecture around the end of this decade. While this technology plan will attract technical interest over then next 4-5 years, it will eventually reduce the number of architectures competing with MIPS by one more.

Microsoft's Windows NT represents a significant destabilizing force in today's PC industry and serves as a potential threat to Intel's business model over the next several years. If Windows NT continues to take hold, and application developers continue to compile their applications for both Intel and the RISC platform (MIPS and Alpha in production today, PowerPC next year), then users will choose their computing platform based on price/performance, rather than on the applications catalog. This should dramatically increase RISC penetration of the PC world. MIPS may be the biggest beneficiary of this change, since it already has the broadest set of CPUs and the most experience on NT. More than 300,000 copies of the Windows NT for MIPS have already shipped as part of Microsoft's standard Windows NT CD distribution. Last year MIPS formed the NT Open Design Center to further accelerate this transition. The ODC concentrates on two development activities -- co-developing system level chipsets and firmware for Windows NT hardware platforms, and supporting application developers in adopting MIPS as one of their Windows NT targets. Already, more than ten different system chipsets support NT-on-MIPS, including portable, multiprocessing, and low-cost systems, with support of ISA, EISA, VESA Local bus, and PCI bus. The combination of 4 pin-compatible CPUs, with this chipset variety gives system makers valuable new opportunities to build differentiated (hence more profitable) system products.

MIPS is more than an interesting partnership business model, it is a well-developed family of mainstream CPUs, a diverse collection of embedded processor devices, a range of commercially available system chipsets, and a mature software base of operating systems, development tools and compilers. Here is a family portrait gallery, describing just a sampling of the present and forthcoming CPUs. A technical overview of the 64b processors follows in Figure 3.

R4400 - The R4400 comes in three flavors, the PC version with low pin count (179 pin) for cost-sensitive systems, the SC version with dedicated, high bandwidth secondary cache, and the MC version, with extensive support of symmetric multiprocessing. At 200 MHz, the R4400 reaches almost 120 SPECint, higher than any other processor at equivalent volume. At the same time, it is manufactured by separate suppliers, IDT, NEC and Toshiba, ensuring rapid price declines. The R4400, like its predecessor, the R4000, implements a full 64b architecture, with flat 64b addressing, 64b integers and support of 64b data types in the compilers.

R4600 - The R4600 is hardware and software compatible with the R4400PC. Its small die size allows aggressive pricing, less than $200 from IDT, Toshiba and NKK. In real Windows NT systems outperforms Pentium 90Mhz by roughly a factor of two, at a lower price. Even compared to PowerPC, it yields better performance at half the chip price. In addition, it implements improved integer multiply latency to accelerate multimedia operations like real-time MPEG decode.

R4200 - The R4200 is completely hardware and software compatible with the R4600 and R4400PC, but takes high performance 64b computing into a new

	R4200	**R4400**	**R4600**	**R8000**
Die size	1 x 75mm^2	1 x 130mm^2	1 x 75mm^2	2x295mm^2
First silicon	Q3 93	Q4 92	Q3 93	Q3 93
System shipment	Q2 94	Q1 93	Q2 94	Q3 94
Volume price	$60-70	$300-$1500	$175-488	>$2000
Clock range	80-100MHz	100-200MHz	100-150MHz	75+MHz
SPECint range	50-65	50-125	75-105	108
SPECfp range	25-38	50-135	50-92	310
On-chip cache	16K/8K	16K/16K	16K/16K,2-way	16K/16K
Off-chip cache	PC-style	256K-4M	PC-style	2M-16M

A note on caches - the R4200, R4400PC and R4600 all have the same multiplexed 64b address data bus. A number of chipsets, especially those for low-cost desktop designs, now support inexpensive secondary caches (128K-2MB)) in the style of 486 PC secondary caches

Figure 3

domain: low-cost, portable applications. It achieves 55 SPECint in performance, yet dissipates less than 2 watts. The simple design and tiny die size (less than that of the 486DX2), has allowed NEC, the initial manufacturer, to price it well below $80. Combined with a low-cost bus converter and cache controller like Toshiba's Tiger-shark, it allows PC companies to easily assemble of machine with the performance of Pentium-60 and the price of a 486SX-25-based system without even a motherboard redesign. Moreover, its small core, integrating integer and floating point capability into a single block, makes it suitable for further aggressive cost reduction. Over the next 12 months, the 4200 die size will shrink by another 2x, allowing a manufacturing cost below $20. This makes it the ideal part for Nintendo's upcoming *Ultra 64* home video game, coming later in 1995.

R8000- The R8000, announced in June, is now shipping in volume. A wide variety of industry-standard benchmarks confirm that this is the fastest supercomputing processor on the planet. The R8000 focuses on the extreme computing requirements of scientific applications, especially data-intensive vector applications traditionally reserved for multi-million dollar supercomputers. It is both first superscalar implementation of the MIPS architecture, and one of the most aggressive superscalar implementations of any architecture. At 75MHz, the two-chip CPU core executes up to four instructions, representing up to six operations, per cycle, for a theoretical sustained bandwidth of 300 million floating point operations per second, the fastest of any announced general-purpose VLSI processor. In addition, it implements a novel "streaming superscalar cache" architecture allowing sustained bandwidth of 1.2GB/s on large data sets (up to 16MB in first-level floating point cached data). This combination of high instruction execution rate, with high sustained data bandwidth allows R8000 to realize more than 75% of the theoretical throughput, even on large problems like 1000x1000 LINPACK. Furthermore, it includes extensive support for cache-coherent symmetric multiprocessing, the key to transparent, compiler-generated parallelization of computation across many CPUs for additional throughput. The impact of R8000can be easily seen in a comparison between Silicon Graphics Power Challenge system, and the most successful of all classical supercomputers, the Cray YMP. Both support large memory, high bandwidth I/O. parallelization across multiple processors, and roughly 300MFLOPS peak throughput per processor. In the Cray, however, each CPU requires hundreds of ECL gate arrays, special cooling arrangements and static RAM memory. Power Challenge uses just the two custom VLSI chips for the CPU, has the power and cooling requirements of a photocopier and uses commodity dynamic RAM memory. Comparable configurations differ by a factor of ten in price. The R8000 outperforms every other microprocessor-based system in a wide variety of scientific benchmarks, including SPECfp92 (310) and LINPACK (265MFLOPs for 1000x1000) for a single processor.

T5 - T5 is the next generation flagship MIPS processor. Like R4400 it is implemented as a single, high-frequency chip, so it can be used in low-cost, high-performance desktops. Like the R4400 is has extensive native support for symmetric multiprocessing. Like R8000, it is aggressively superscalar, allowing high floating point performance. Like R8000, it continues to innovate in cache architecture, allowing high sustained throughput even on data sets that overwhelm the on-board caches. The first T5 parts will be built around the end of the year, with volume system shipments in second half of 1995. According to detailed simulations, it will well exceed 250 SPECint and 350 SPECfp even in its initial version. Despite the big step in performance, T5 maintains complete binary compatibility for applications from R3000, R4000 and R8000 systems.

MR300 - The MR300 series from HDL Systems represents the opposite end of the computing spectrum from chips like R8000. HDL has used MIPS's R3000 design to create a compatible and completely synthesizable processor core. Because it is written in VHDL, it is simple for the user to add application-specific features, thoroughly simulate the design, and generate a new physical implementation in almost any process technology. The combination of the simplicity of the MIPS architecture and HDL's own optimization methods allows the processor core to be implemented in less than 10 square mm. According to Microprocessor Report's cost model, this means the CPU core would add less than one dollar to manufacturing cost of an embedded system chip. HDL has demonstrated the flexibility of its approach by releasing five initial variants, including versions with embedded debug support, with enhanced interrupt support, and with digital signal processing acceleration. By starting from the MIPS design, HDL offers a unique capability for embedded processor cores, yet maintains compatibility with compilers, debuggers, real-time operating systems, emulators, prototyping boards and other development tools

MIPS operates in wider range of markets than its parent, Silicon Graphics, but MIPS and Silicon Graphics are strongly interdependent. Silicon Graphics uses only about 5% of the total MIPS chip volume, but it benefits in two ways from the proliferation of MIPS in the diverse markets of UNIX technical and commercial computing, Windows NT PCs, embedded control and entertainment. First, the success of MIPS drives up the volume of MIPS parts and drives down the prices paid by every adopter. The success of MIPS seals the commitment of the semiconductor partners to the MIPS architecture business and ensures the availability of the best and fastest fabrication technology for building the high-performance MIPS CPUs needed by Silicon Graphics. Second, the price, performance and functionality of MIPS carries the technology into important new domains that Silicon Graphics cannot directly address with UNIX workstations and servers. Nintendo, for example, has adopted the MIPS architecture and Silicon Graphics 3D graphics technology for its next generation of arcade and home video games. With 35M home game units already in place, this one market represents a potential volume of 40-100M MIPS processors over the next decade. This rivals the size of the Intel-based PC market.

MIPS also benefits from the success of Silicon Graphics. Silicon Graphics is the hottest computer company in the market today, a $1.5B revenue run rate, with 35% average annual growth, 13% operating profit, and enormous visibility due to key relationships with leaders in information superhighways (US National Information Infrastructure project), interactive video communications (key technology supplier to Time Warner Cable), home entertainment (Nintendo), and Hollywood (systems partner for Industrial Light and Magic, animator of "Jurassic Park", "Terminator 2" and other major films). In fact, investor confidence in Silicon Graphics growth, profitability, consistency and technological assets has pushed the market value of Silicon Graphics to about $4B, higher than that of Sun Microsystems or Apple Computer, and approaching that of Digital. This financial strength ensures that MIPS and Silicon Graphics will have the resources to continue to push processor performance and proliferation, and that a wide range of applications will seek out MIPS and Silicon Graphics for a competitive advantage.

Applications: Windows NT on MIPS

Here is a sample of some of the hundreds of software packages already offered by third parties for Windows NT on MIPS platforms (availability now or within six months):

AGE Logic Inc.	XoftWare/32
Ampersand	Matrix
Congruent	ToolBuster
Conner Software	Backup Exec
Consensys Corp.	Unite!
DEC	Excursion
Dyad Software	M++4.0
Executive Software	File Alert
Graphitti Software	Open Draw Professional
GrayTech Software	CAD X11
GrayTech Software	CAD X11/Lite
Hamilton Laboratories	Hamilton C Shell
Intusoft	ICAP/4NT
Ithaca	Hoops
Kenan Technologies	Acumate ES
Macromedia	MacroMode/NT
Massteck	MAX ROUTE
Media Vision	OpenGL SDK
Microsoft	C/C++
Microsoft	Mail
Microsoft	Schedule+
Microsoft	SQL Server
Mozart	Scraperware
NetManage	Chameleon32 v3.11
Parametric Technologies	Pro/ENGINEER
Platinum Software	SeQueL to Platinum
SunSelect	NT PC-NFS
SQL Business Systems	SQLstor
Visual Numerics	PV-Wave Advantage
Welcom Software	Texim Project 2.0
Absoft	Absoft FORTRAN77
Arbor Software	eSSbase
AccuSoft	Image Format LibraryCin-
com	Supra Server
Computervision	Design View
Edinburgh Portable Compilers	FORTRAN77
FSIC Associates	ProfitFinder
Hummingbird	eXceed/NT
IMRS	Hyperion
LBMS	Process Engineer4
Massteck	MAX EDS
Microsoft	Excel
Microsoft	SNA Server
Microsoft	Visual C++
NeTpower	NeTexecute
NeTpower	NeTcompile
Pixar	Typestry 2.0
SSA	Plan Assistant
SSA	Formula Assistant
SSA	Financial AssistantSummit
Software	BasicScript
Wall Data	Rumba
Wolfram	Mathmatica
Wonderware	Intouch

Hardware Sources

System platforms for Windows NT on MIPS are available in Europe from the following sources.

Acer

Contact:Wim Van Seters
Hastelweg 250
Eindhoven 5652 CN
The Netherlands
tel +31 40 50 1234
fax +31 40 52 9124

Deskstation Technology

Contact:Mark Lewis
James House
27/35 London Road
Newbury, Berkshire RG13 1JL
England
tel +44 773 829 542
fax +44 773 820 206

Siemens Nixdorf

Contact:Patrick Le Lannic
Siemens Nixdorf Informations Systems
Centre Industriel
15, rue Decartes
B. P. 83
78371 Plaisir Cedex - FRANCE
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fax +33 1 34 81 10 96

ShaBLAMM! Computer Corporation

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Shuttle Computer

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Dilog

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GETEK

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Other important soruces:

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MIPS-based systems for UNIX are available from Silicon Graphics, Siemens Nixdorf, Tandem, Pyramid, Concurrent Computer and Dansk Data Elektronik, through sales organizations in all major European countries.

Windows NT Update

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