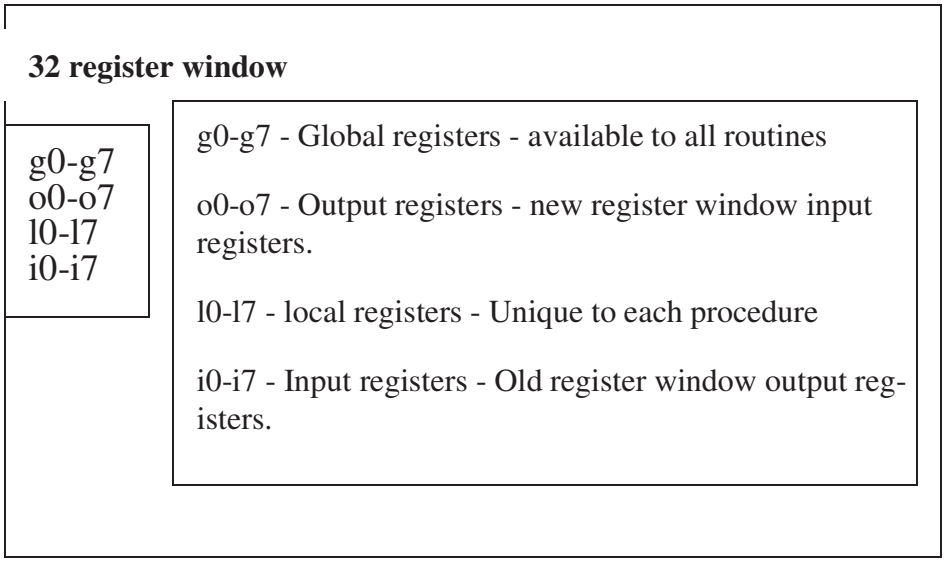
Fig 2a.

Sparc Registers

Sparc Version 8 architecture can have anywhere between 40 and 520 general purpose 32 bit registers. A routine can only access 32 of these registers at one time. 8 of these are globals and available at all times [%g0 - %g7]



PC - Program Counter - current instruction being executed.

nPC - next Program Counter - address of next expected instruction (pipelining + delayed transfer control)

PSR - Processor Status Register

TBR - Trap base register - contains 3 fields that (when concatenated) point to the address where control is transferred whan a trap occurs.

WIM - Window Invalid Mask - (32 bit register like others) one bit for each possible window.

Y - Multiply / Divide Register - 32 bit by 32 bit multiplication and division can produce 64 bit results - most significant bits stored in Y register.

ASR and DTP - not used on most implementations.